UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,592	03/19/2004	Jack B. Andersen	D2A1180-1	9248

7590 08/04/2005

Law Offices of Mark L. Berrier
Bldg. II, Ste. 216
1250 Cap. of Texas Hwy. S.
Austin, TX 78746

EXAMINER	
NGUYEN, HIEU P	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

ST

Office Action Summary	Application No.	Applicant(s)	
	10/805,592	ANDERSEN ET AL.	
	Examiner	Art Unit	
	Hieu Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-15* is/are allowed.

6)☒ Claim(s) *1-7,11* is/are rejected.

7)☒ Claim(s) *8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1 & 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melanson (US 6294954) in view of El-Hamamsy (US 5118997).

Regarding claim 1,Fig. 1 & 2 of Melanson shows a system comprising: a pulse width modulation (PWM) controller, wherein the PWM controller (101) provides a first output for a high-side PWM signal and a second output, wherein the output stage is configured to receive the high-side signal from the first PWM controller output and the low-side signal from the second PWM controller output.

Melanson discloses the claimed invention except for "the high-side signal is coupled to a high-side transistor through a pulse transformer." However, Fig. 1 of El-Hamamsy shows a system having two out-of phase signals, and one of the signals is a high-side signal, which is coupled to high-side transistor through a pulse transformer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of El-Hamamsy into the circuit of Melanson by having a pulse transformer between the high-side signal and high-side transistor. The ordinary artisan would have been motivated to modify the circuit of Melanson in the manner set forth above for at least the purpose of optimizing the performance of the amplifier.

Regarding claim 6, Fig. 2 of Melanson indicates the PWM controller (101) is configured to produce a pulse as the high-side signal at the first PWM controller output (upper signal).

Regarding claim 7, Melanson and El-Hamamsy disclose everything claimed, as applied above. In addition, Fig. 1 of El-Hamamsy discloses the output stage further comprises a low-voltage driver (18), and wherein the low-voltage driver amplifies the pulse and transmits the amplified pulse to the pulse transformer (22). . It would have been obvious to one having ordinary skill in the

art at the time the invention was made to incorporate the teaching of El-Hamamsy into the circuit of Melanson by having a pulse transformer between the high-side signal and high-side transistor. The ordinary artisan would have been motivated to modify the circuit of Melanson in the manner set forth above for at least the purpose of optimizing the performance of the amplifier.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melanson and El-Hamamsy in further view of Takina (US 6064259).

Regarding claim 2, Melanson and El-Hamansy disclose everything claimed. In addition, Fig. 9 of Melanson disclose a system further comprising a high-side delay unit (902) configured to delay the high-side signal by a first programmable amount and a low-side delay unit (903) configured to delay the low-side signal by a second programmable amount.

Melanson fails to disclose the delay unit is programmable. However, Fig. 2 of Takina discloses a PWM amplifier having a programmable delay unit (245).

It would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teaching of Takina into the system of Melanson and El-Hamamsy by upgrading to programmable delay unit. The ordinary artisan would have been motivated to modify the amplifier of Melanson in the manner set forth above for at least the purpose of precisely controlling the dead time.

Regarding claim 3, Melanson and El-Hamamsy disclose everything claimed, as applied above. But Melanson and El-Hamamsy fail to disclose that the delay units are integrated into the PWM controller. However, Takina further discloses [Fig. 12; col.7, lines 67 and col.8, line 1] the high-side programmable delay unit and the low-side programmable delay unit (U39 and U40) are integrated into the PWM controller.

It would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teaching of Takina into the system of Melanson and El-Hamamsy by integrating the delay units into the PWM controller. The ordinary artisan would have been motivated to modify the amplifier of Melanson and LE-Hamamsy in the manner set forth above for at least the purpose of reducing the size of the system.

Regarding claim 4, Melanson and El-Hamamsy disclose everything claimed, as applied to claim 2. Melanson further discloses [col. 2, lines 18-22] the delay unit (delay element) is either a digital or an analog delay. But Melanson fails to disclose the unit is programmable. However, Takina discloses a delay unit is programmable as applied to claim 3.

It would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teaching of Takina into the system of Melanson and El-Hamamsy by having a digital programmable delay unit. The ordinary artisan would have been motivated to modify the circuit of Melanson and

El-Hamamsy in the manner set forth above for at least the purpose of minimizing maintenances and noise (easier to calibrate and adjust and resistance to noise).

Regarding claim 5, Melanson and El-Hamamsy disclose everything claimed, as applied to claim2. In addition, Fig. 9 of Melanson discloses the PWM controller is configured to adjust overlap of pulses of the high-side signal and the low-side signal by adjusting at least one of the first and second programmable amounts (amounts are controlled by Dead Time Control 901).

Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Melanson and El-Hamamsy in further view of Mazda (US Pub. 2004/0036533).

Regarding claim 11, Melanson and El-Hamamsy disclose everything claimed, as applied to claim 2. But they fail to disclose the system wherein "the low-side signal is coupled to a low-side transistor through one or more level shifting capacitors". However, Fig. 1 of Mazda shows a switching amplifier having the low-side signal is coupled to a low-side transistor through a level shifting capacitors (Cc). It would have been obvious to on having ordinary skill in the art at the time the invention was made to incorporate the teaching of Mazda by using one or more shifting capacitors disposed at the low side signal. The ordinary artisan would have been motivated to modify the system of Melanson and El-Hamamsy in the manner set forth above for at least the purpose of obtaining DC isolation [0013].

Allowable Subject Matter

Claims 12-15 are allowed.

Claim 8-10 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8-10, the prior art of record fails to disclose or suggest a structure of a PWM controller comprising "the output stage further comprises a third transistor, wherein the third transistor is coupled to receive the low-side signal and wherein the third transistor is configured to turn of the high-side transistor when the low-side signal is asserted" in combination with the rest of the limitations of the claim(s).

Claims 12-15 are allowed over prior art because none of the prior art disclosed or suggested showing the particular structure and/or operation recited in these claims namely:

Claims 12-15 call for, among others, "a third transistor (Q1) coupled between the second input and the first transistor".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 571-272-0218. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zandra V Smith
Primary Examiner

hn